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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,564	LLOYD, STACEY G.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 7-19 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 8/6/2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-5, 8-9, 11-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al, (U.S. 5,796,972), in view of Handy ("The Cache Memory Book", 2nd ed.), in view of Dockser (U.S. 6,006,030).

5. As per claim 1:

Johnson disclosed a method for handling operations within a hardware device, comprising:

Providing within the device information regarding an operation, the operation having a predetermined responsive output as encoded within a transaction lookup table (Fig. 8, Ucode ROM 294) and an alternative responsive output stored in a register (Fig. 8, Patch RAM 296), the provided information including information identifying the operation: [(The predecode block 290 provides identifying information for each operation. Col. 11, line 62 to col. 12, line 18. The ROM 294 is given an address and

outputs the predetermined operation to a multiplexer 298. The Ram 296 contains alternative operations, and supplies them to the multiplexer 298.]

Selecting at least some of the identifying information of the operation to output to the transaction lookup table, and output of the transaction lookup table are input into a multiplexer: [Figs. 8 & 10, the identifying information is provided to the Ucode ROM 294 via line 358 and the output of the Ucode ROM 294 is output to the multiplexer 298.]

Selecting the alternative responsive output for the operation instead of the predetermined responsive output based upon the identifying information and directing the multiplexer to output the alternative responsive output, such that the multiplexer effectively converts at least some of the information regarding the operation based upon the selected identifying information: [Based on the identifying information, the ID RAM produces a CS RAM SEL bit on line 362 which indicates which output to choose, the ROM or RAM (lookup table or alternative register). See figs. 8 and 10, col. 11, line 62 to col. 12, line 33 and co. 13, line 3-17.]

And executing the operation based upon the converted information: [The instructions are forwarded on the output of the multiplexer to execution units. (Figures 4 and 8)]

Johnson fails to teach a comparator, wherein the output of the comparator provides an input to the multiplexer. Johnson instead teaches the ID RAM as a index-able memory, wherein the pre-decode unit 290 provides an indexing address, and the ID RAM further converts this into another address for the ROM or RAM and also provides an associated CS RAM SEL bit.

However, Handy teaches that CAM memories are well known in the art and are a different method of lookup table memories. Instead of providing an address as an input, a data input is provided, which is then compared against a stored value. When a match is present, the corresponding stored data is output. Implementing the ID RAM as a CAM memory instead of an indexed memory would cause the identifying information to be provided to a comparator and some of the decoded identifying information would still be provided to the UCODE ROM 294. The output of the comparator (The CAM memory as a whole performs comparisons, and therefore is a comparator) would consist of a CS RAM SEL bit, which results from a match and is input to the multiplexer to select from which memory, the predetermined (ROM 294) or the alternative (RAM 296), the output is to be selected from. (Handy, pages 14-18)

It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to index-able memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is input to the memory, and the associated data is retrieved, in both the index-able memory and the CAM memory.

Johnson and Handy failed to teach by employing a masking register that filters the at least some of the identifying information of the operation for output to the comparator, the masking register being logically AND'ed with all the identifying

information of the operation and having binary ones corresponding to the at least some of the identifying information to output to the comparator and binary zeros corresponding to other of the identifying information not output to the comparator.

However, Dockser disclosed by employing a masking register that filters the at least some of the identifying information of the operation for output to the comparator, the masking register being logically AND'ed with all the identifying information of the operation and having binary ones corresponding to the at least some of the identifying information to output to the comparator and binary zeros corresponding to other of the identifying information not output to the comparator (Dockser: Figure 1 element 50, column 5 lines 20-45)(The list contains the instructions not to be implemented and mask registers to mask out certain bits. It's obvious to one of ordinary skill in the art that an AND operator could be used for masking out the bits not to be considered. The result is then compared to incoming instructions for matches.).

The advantage of using a masking register is that it allows for the relevant bits to pass through and the irrelevant bits to be ignored (Dockser: Column 5 lines 35-39). One of ordinary skill in the art would have been motivated by this advantage to implement a mask register to only allow the relevant bits for a matching instruction to pass through to a comparator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a mask register to get rid of irrelevant bits for the advantage of making the comparison easier to detect the correct instructions.

6. As per claim 2:

Johnson, Handy, and Dockser disclosed the method of claim 1, wherein the provided information is within a register of the device: [The predecode block 290 provides information for each operation. Col. 11, line 62 to col. 12, line 18. It comes from an entry in the memory unit (instruction memory 252), which is a register within the device.]

Furthermore, although Johnson, in view of Handy, does not specifically teach pipeline latches, Examiner takes Official Notice that pipeline latches (registers) between stages in a processor are very well known and allow proper timing between combinational logic stages, such as the fetching, predecoding, decoding, execution, etc. Specifically teaching pipeline registers would cause there to be a register between the different stages of the pipeline, including between the memory and decode stages, and thus, the provided information would be within a register of the device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include pipeline latches (registers) between stages since Examiner takes Official Notice that pipeline latches allow proper timing between stages in a pipelined processor and are well known in the art.

7. As per claim 3:

Johnson, Handy, and Dockser disclosed the method of claim 1, wherein the identifying information is within a register of the device: [The predecode block 290 provides identifying information for each operation. Col. 11, line 62 to col. 12, line 18. It comes from an entry in the memory unit (instruction memory 252), which is a register within the device.]

Furthermore, although Johnson, in view of Handy, does not specifically teach pipeline latches, Examiner takes Official Notice that pipeline latches (registers) between stages in a processor are very well known and allow proper timing between combinational logic stages, such as the fetching, predecoding, decoding, execution, etc. Specifically teaching pipeline registers would cause there to be a register between the different stages of the pipeline, including between memory and decode stages, and thus, the provided information would be within a register of the device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include pipeline latches (registers) between stages since Examiner takes Official Notice that pipeline latches allow proper timing between stages in a pipelined processor and are well known in the art.

8. As per claim 4:

Johnson, Handy, and Dockser disclosed the method of claim 1, wherein the converted information is within a register of the device: [The converted information is stored in an entry in the RAM 296. An entry in the RAM 296 is a register in the device. Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

9. As per claim 5:

Johnson, Handy, and Dockser disclosed the method of claim 1, wherein the step of providing information regarding the operation comprises providing the predetermined responsive output and the alternative responsive output: [The RAM 296 outputs the alternative responsive output and the ROM 294 outputs the predetermined responsive output. Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

10. As per claim 8:

Johnson disclosed a method for redirecting transactions [instructions] within a hardware device, wherein transactions occurring within said device contain fields of information regarding the transaction [inherently, the instructions contain fields of information], the method comprising the steps of:

Loading all of said fields necessary to identify a transaction into a first register: [The entries within Instruction Memory 252 contain instructions (inherently loaded), and since they can be decoded and executed, the instructions inherently include all of the fields necessary to identify the instructions. Fig. 7, col. 1, line 62 to col. 12, line 18.]

Selecting which fields of said first register are to be acted upon and inputting the selected fields into a multiplexer: [Johnson teaches using the opcode as an index into the ID RAM. Therefore there is a selection of the index field of an instruction from the first register (an entry in memory).]

Converting the transaction information to be redirected through a pre-programmed value for each said field by inputting into the multiplexer a predetermined responsive value into the multiplexer, the predetermined responsive value stored in a transaction lookup table and an alternative responsive output stored in a register, the multiplexer also receiving input such that the multiplexer outputs the alternative responsive value for the transaction based upon the ID RAM's selecting output, CS RAM SEL. Fig. 8, 10, col. 11, line 62 to col. 12, line 33.]

Johnson teaches the ID RAM as a index-able memory, wherein the pre-decode unit 290 provides an indexing address, and the ID RAM further converts this into another address for the ROM or RAM and also provides an associated CS RAM SEL bit. Therefore, Johnson fails to teach the multiplexer also receiving input from *a comparator*, such that the multiplexer outputs the alternative responsive value for the transaction based upon *the comparator comparing the selected fields to the transaction resulting in a match*. Johnson further fails to teach the output from the multiplexer (Examiner's interpretation of "said new transaction results") is sent to a register.

However, Handy teaches that CAM memories are well known in the art and are a different method of lookup table memories. Instead of providing an address as an input, a data input is provided, which is then compared against a stored value. When a match is present, the corresponding stored data is output. Implementing the ID RAM as a CAM memory instead of an indexed memory would cause the identifying information to be provided to a comparator and some of the decoded identifying information would still be provided to the UCODE ROM 294. The output of the comparator (The CAM memory as a whole performs comparisons, and therefore is a comparator) would consist of a CS RAM SEL bit, which results from a match and is input to the multiplexer to select from which memory, the predetermined (ROM 294) or the alternative (RAM 296), the output is to be selected from. (Handy, pages 14-18)

It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to index-able memories and allows any entry to

point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is input to the memory, and the associated data is retrieved, in both the index-able memory and the CAM memory.

Furthermore, although Johnson, in view of Handy, does not specifically teach pipeline latches, Examiner takes Official Notice that pipeline latches (registers) between stages in a processor are very well known and allow proper timing between combinational logic stages, such as the fetching, predecoding, decoding, execution, etc. Specifically teaching pipeline registers would cause there to be a register between the different stages of the pipeline, including between the decode stages and the execution, and thus, the outputted results from the multiplexer 298 would be sent to a register.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include pipeline latches (registers) between stages since Examiner takes Official Notice that pipeline latches allow proper timing between stages in a pipelined processor and are well known in the art.

Johnson and Handy failed to teach the fields of said first register selected by employing a masking register that filters the fields of said first register, the masking register being logically AND'ed with the said first regiser and having binary ones corresponding to the fields being selected and binary zeros corresponding to the fields not selected.

However, Dockser disclosed the fields of said first register selected by employing a masking register that filters the fields of said first register, the masking register being logically AND'ed with the said first regiser and having binary ones corresponding to the fields being selected and binary zeros corresponding to the fields not selected (Dockser: Figure 1 element 50, column 5 lines 20-45)(The list contains the instructions not to be implemented and mask registers to mask out certain bits. It's obvious to one of ordinary skill in the art that an AND operator could be used for masking out the bits not to be considered. The result is then compared to incoming instructions for matches. The list is a memory that isn't specified, but it's obvious to one of ordinary skill in the art that the list could be registers for the advantage the list being accessible quicker than other memories.).

The advantage of using a masking register is that it allows for the relevant bits to pass through and the irrelevant bits to be ignored (Dockser: Column 5 lines 35-39). One of ordinary skill in the art would have been motivated by this advantage to implement a mask register to only allow the relevant bits for a matching instruction to pass through to a comparator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a mask register to get rid of irrelevant bits for the advantage of making the comparison easier to detect the correct instructions.

11. As per claim 11:

Claim 11 essentially recites the same limitations of claim 1. Therefore, claim 11 is rejected for the same reasons as claim 1.

12. As per claim 12:

Johnson, Handy, and Dockser disclosed the method of claim 11, wherein the step of creating a list of identified operations includes first loading transaction identification: [The list of identified operations is stored in the ID RAM (Fig. 8, 10 of Johnson), which, in view of Handy, is a CAM memory (see Handy, pages 14-18). The CAM memory ID RAM is inherently loaded with the list, or the CAM memory ID RAM would not contain any data.]

13. As per claim 14:

Claim 14 essentially recites the same limitations of claim 1. Therefore, claim 14 is rejected for the same reasons as claim 1.

14. As per claim 15:

Johnson, Handy, and Dockser disclosed the system of claim 14, wherein one or more of said storage means may be selectively enable or disabled: [From one point of view, the MUX effectively causes an enabling or disabling of the Ucode ROM 294 and Patch RAM 296. From another point of view, the address that indexes into the RAM 296 and ROM 294 causes an enabling of an entry of the RAM 296 and ROM 294 and a disabling of the rest of the entries in the RAM 296 and ROM 294. Fig. 8, col. 11, line 62 to col. 12, line 33.]

15. As per claim 16:

Johnson disclosed in a data processing system utilizing a hardware control device in which a given operation results in a predetermined response for that

operation, a system for providing a programmable redefinition of allowed instructions and associated responses within said hardware device including:

First register means which contains fields to identify preselected operations which may occur within the system: [The Instruction Memory contains instruction in entries (registers) and contains identifying information which is decoded to indicate operations. Fig. 8]

Second register means which operates upon selected fields in the first register means to further define a criteria for which redirecting a response is desired: [ID RAM 352 contains multiple registers. They operate on the first register means' selected field that is input (figs. 8 & 10) by interpreting it and outputting further defined criteria for redirecting a response. Col. 11, line 62 to col. 12, line 33.]

Transaction lookup table means to output a standard value for the current operation: [Ucode Rom 294 contains the standard values. Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

And multiplexer means receiving input indicating the desired selection (via line 302), transaction lookup table means (via line 293) and outputting a substitute value for a predetermined value the current operation [when the CS RAM SEL bit selects the Patch RAM 296, the substitute value replaces the predetermined value], the substitute value stored in a register (Patch RAM 296) and the predetermined value stored in a transaction lookup table (Ucode ROM 294): [Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

Johnson failed to teach the multiplexer also receiving input from *a comparator* means that is used for selecting an input of the MUX for output. Instead, Johnson teaches the ID RAM as a index-able memory, wherein the pre-decode unit 290 provides an indexing address, and the ID RAM further converts this into another address for the ROM or RAM and also provides an associated CS RAM SEL bit.

However, Handy teaches that CAM memories are well known in the art and are a different method of lookup table memories. Instead of providing an address as an input, a data input is provided, which is then compared against a stored value. When a match is present, the corresponding stored data is output. Implementing the ID RAM as a CAM memory instead of an indexed memory would cause the identifying information to be provided to a comparator and some of the decoded identifying information would still be provided to the UCODE ROM 294. The output of the comparator (The CAM memory as a whole performs comparisons, and therefore is a comparator) would consist of a CS RAM SEL bit, which results from a match and is input to the multiplexer to select from which memory, the predetermined (ROM 294) or the alternative (RAM 296), the output is to be selected from. (Handy, pages 14-18)

It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to index-able memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is

input to the memory, and the associated data is retrieved, in both the index-able memory and the CAM memory.

Johnson and Handy failed to teach the second register means being a masking register that filters the selected fields of the first register means, the masking register being logically AND'ed with all the fields of the first register means and having binary ones corresponding to the selected fields and binary zeros corresponding to other of the fields.

However, Dockser disclosed the second register means being a masking register that filters the selected fields of the first register means, the masking register being logically AND'ed with all the fields of the first register means and having binary ones corresponding to the selected fields and binary zeros corresponding to other of the fields (Dockser: Figure 1 element 50, column 5 lines 20-45)(The list contains the instructions not to be implemented and mask registers to mask out certain bits. It's obvious to one of ordinary skill in the art that an AND operator could be used for masking out the bits not to be considered. The result is then compared to incoming instructions for matches. The list is a memory that isn't specified, but it's obvious to one of ordinary skill in the art that the list could be registers for the advantage the list being accessible quicker than other memories.).

The advantage of using a masking register is that it allows for the relevant bits to pass through and the irrelevant bits to be ignored (Dockser: Column 5 lines 35-39). One of ordinary skill in the art would have been motivated by this advantage to implement a mask register to only allow the relevant bits for a matching instruction to

pass through to a comparator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a mask register to get rid of irrelevant bits for the advantage of making the comparison easier to detect the correct instructions.

16. As per claim 17:

Claim 17 essentially recites the same limitations of claim 15. Therefore, claim 17 is rejected for the same reasons as claim 15.

17. As per claim 18:

Claim 18 essentially recites the same limitations of claim 1. Therefore, claim 18 is rejected for the same reasons as claim 1.

18. Claims 7, 10 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al, (U.S. 5,796,972), in view of Handy ("The Cache Memory Book", 2nd ed.), in view of Dockser (U.S. 6,006,030), further in view of ("The PowerPC Architecture: A specification for a new family of RISC processors").

19. As per claim 7:

Johnson and Handy disclosed the method of claim 5.

Johnson and Handy failed to teach what makes up the operation identifications. Johnson and Handy disclosed using a CAM memory in place of the ID RAM of Johnson (fig. 10, item 352); however, it is not specified what information identifies an operation since the instruction set is not defined

However, the PowerPC Architecture has taught operation identifications in instructions comprising fields for operation identification (OPCD field, PowerPC, page 21), length (L field, PowerPC, page 21), attribute field (RA field, PowerPC, page 22),and target (BF field, PowerPC, page 19) of each operation. One of ordinary skill in the art would have recognized that using the PowerPC Architecture as the architecture in the method/apparatus of Johnson, in view of Handy, would be beneficial given the expansive software base that is compatible with the PowerPC architecture. Using an architecture with such a wide acceptance in the field allows for the method/apparatus to run a wide variety of programs. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the PowerPC architecture in the method/apparatus of Johnson, in view of Handy, in order to provide an established instruction set with an expansive collection of compatible software programs.

20. As per claim 10:

Claim 10 essentially recites the same limitations of claim 7. Therefore, claim 10 is rejected for the same reasons as claim 7.

21. As per claim 13:

Claim 13 essentially recites the same limitations of claim 7. Therefore, claim 13 is rejected for the same reasons as claim 7.

22. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al, (U.S. 5,796,972), in view of Handy ("The Cache Memory Book", 2nd ed.), in view of

Dockser (U.S. 6,006,030), further in view of IBM Technical Disclosure Bulletin, Vol. 37, No. 03.

23. As per claim 19:

Johnson and Handy disclosed the system of claim 18.

Johnson and Handy failed to teach wherein the comparator is responsive to a mask of the identifying information. Johnson is silent on the specific identifying information, and only teaches that a decoded instruction address is provided (col. 11, line 62 to col. 12, line 9). Furthermore, Johnson, in view of Handy, teaches comparing identifying information of an instruction in a CAM style memory ID RAM, but again, there is no specific teaching as to what the identifying information is exactly made up of.

IBM teaches only sending the opcode as identifying information, and therefore masking the remaining portions of the instruction, when deciding whether or not an instruction needs to be substituted. (See figure in upper-right hand corner).

It would have been obvious to one of ordinary skill in the art to mask the identifying information of the instruction to select only the opcode to be send to the CAM memory, ID RAM, since an opcode's purpose is to identify instructions and since IBM explicitly teaches masking instruction information to produce only an opcode for identifying purposes.

Response to Arguments

24. The arguments presented by Applicant in the response, received on 8/8/2006 are considered persuasive.

25. Applicant argues "Johnson and Handy failed to teach by employing a masking register that filters the at least some of the identifying information of the operation for output to the comparator, the masking register being logically AND'ed with all the identifying information of the operation and having binary ones corresponding to the at least some of the identifying information to output to the comparator and binary zeros corresponding to other of the identifying information not output to the comparator" for claims 1, 8, 11, 14, 16, and 18.

This argument is found to be persuasive for the following reason. The examiner agrees that Johnson and Handy failed to teach a masking register that filters some of the identifying information that is input into the comparator. However, due to the amendment, a new ground of rejection has been given.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100